Next-Generation Ultra-Fast Signal Synthesis and Sampling

Furaxa has developed a novel method for ultra-fast, highly repeatable signal synthesis and sampling. Based on the patented Libove Gate architecture, the Furaxa sampler/pulser enjoys significant performance and cost advantages over conventional sampler/pulser technology. The innovative circuit architecture provides:

- 4x as many apertures per cycle versus conventional sampling/pulsing technologies
- 16x the repetition rate of conventional sampling/pulsing technologies
- 8x performance of closest competing sampler/pulser circuit
- Unparalleled noise rejection and immunity to control signal imperfections
- Dynamic modulation of amplitude, position and duration of aperture/pulse
- Easy integration into large arrays of matched samplers/pulsers
- Superior stability across all monolithic IC processes

The combined aperture speed, stability and precision coupled with the circuit's compact, parallelizable architecture facilitates simple integration of large numbers of ultra-fast samplers or pulsers on a single IC. Such an array of samplers permits continuous, precise multi-GHz sampling of high-speed microwave signals at multiple points per cycle. Similarly, a pulser array can directly synthesize a tailored microwave waveform using a series of sequentially activated pulse generators.

The exceptional set of performance characteristics of the Furaxa sampler/pulser makes it uniquely suited for applications in advanced test and measurement instrumentation, ultra wideband (UWB) communications, high speed analog signal processing, high speed digital applications and advanced optical communications.

Sampler/Pulser Technology Review

To fully appreciate the superior performance characteristics of the Libove Gate it is helpful to compare the circuit with conventional sampler/pulser technology. Since, any sampling circuit can be simplified to a pulser, we will discuss the two topics of sample generation and pulse generation under the umbrella of aperture generation. Various methods of creating ultra-fast apertures exist. The large majority of methods utilize an architecture that incorporates either a Gilbert Multiplier or a Schottky Bridge. The following matrix reviews the performance that can generally be achieved with each of these elements as compared to the Libove Gate.

	Libove Gate Circuit	Gilbert Multiplier + SRD	Schottky Bridge + SRD
Apertures/Pulses per Cycle	• 4	• 1	• 1
Repetition Rate	• 4+GHz	• Limited to ~250 MHz	• Limited to ~250 MHz
Aperture Width	• ~ 20 picoseconds in GaAs	• ~ 20 picoseconds in GaAs	• ~ 10 picoseconds in GaAs
Aperture Figure of Merit (Rep. Rate / Aperture Width)	• Relative measure - 1.00 • Absolute measure - $2x10^{-4}$	• Relative measure - 0.0625 • Absolute measure - $1.25x10^{-5}$	• Relative measure - 0.125 • Absolute measure - $2.5x10^{-5}$
Monolithic Matched Array	• 64 matched samplers per IC • < 1% mismatch	• Poor SRD matching • High SRD power requirements	• Poor SRD matching • High SRD power requirements
Dynamically Programmable	• Amplitude • Duration • Position	• Difficult on large scale	• Difficult on large scale
Noise Level	• Excellent noise rejection • Low 1/f noise	• Prone to SRD jitter	• Prone to SRD jitter
Signal Imperfections Tolerance	• Immune to control signal imperfections	• Susceptible to control signal imperfections	• Immune to control signal imperfections
Stability	• Superior stability across IC processes and temperature variation • Highly tolerant of large voltage inputs	• Limited stability due to SRD temperature and mismatch constraints	• Limited stability due to SRD temperature and mismatch constraints • Easily damaged with high voltage input

Strengths and Limitations of Conventional Technology

A method that incorporates the Gilbert Multiplier (Figure 1) applies an external sampling control pulse to one set of terminals to create the aperture, while the input signal to be sampled is applied to a second set of terminals. The transistors are forward biased, and the resulting output is proportional to the product of the two signals. This circuit has good input impedance characteristics and can be implemented as a monolithic circuit.

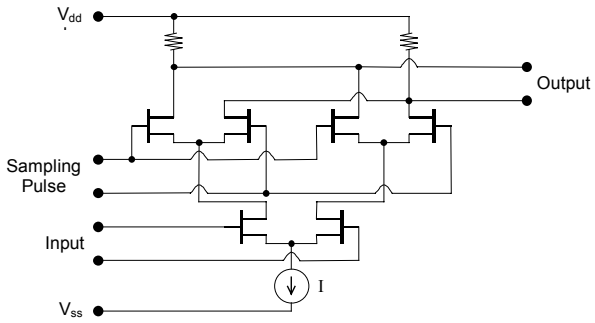

Figure 1 – Gilbert Multiplier

However, a Gilbert Multiplier circuit requires both the rising and falling edge of a control pulse to define the aperture thereby creating a larger aperture width than alternative techniques. Additionally, imperfections in the control pulse, such as ringing, are seen in the output waveform since there is no "noise margin". The input control pulse is multiplied directly by the input signal and must be nearly perfect before, during and after the desired sampling window - placing very stringent requirements on the control signal.

A second method (Figure 2) of generating an ultra-fast aperture incorporates a step recovery diode (SRD) and two or more Schottky diodes. The SRD is charged by applying a forward bias and then is strongly reverse-biased. After the junction charge depletes, the voltage across the SRD changes rapidly creating a sharp, fast transition edge. The edge is then differentiated by capacitors C_1 and C_2 to briefly forward bias the Schottky diodes D_1 and D_2 for a few picoseconds, thereby creating a sampling aperture. This method can create very narrow (as little as a few picoseconds) aperture widths because it relies on a single signal transition (the SRD step pulse.)

However, the SRD-based circuit suffers from jitter and variations in pulse position with temperature fluctuation. Additionally, the SRD requires several nanoseconds to charge and discharge, limiting the pulse-repetition rate of the circuit to approximately 250 MHz. Furthermore, the variable input impedance of the Schottky diodes is sub-optimal for impedance matching making it difficult to fabricate the SRD, capacitors and Schottky diodes in a monolithic design. Finally, the circuit can be easily damaged by overvoltage to the input.

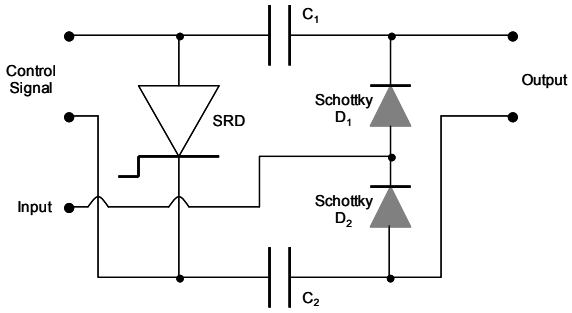

Figure 2 – Step Recovery Diode Circuit

Profile of Furaxa Technology

The Furaxa sampler/pulser represents a leap forward in aperture generation technology with at least an 8x improvement in performance† and a 16x improvement in the repetition rate of the nearest competing technology. The Libove Gate can generate 20 picosecond apertures at 2 gigasamples/second in GaAs. In addition, the unique circuit architecture provides:

- Unparalleled noise rejection and immunity from control signal imperfections
- Dynamic control of the amplitude, position and duration of the sample/pulse
- Minimal jitter and kick-out voltage
- High signal and control input impedances
- Easy integration into large arrays of matched samplers/pulsers
- Fully differential inputs and outputs

The Libove Gate uses a control signal ($V_{Control}$), in conjunction with a level-activated switch gate, to produce both the initiation and extinction of an aperture as illustrated in Figure 3. The sampler/pulser circuit moves through three operational states as $V_{Control}$ falls from an initial voltage that is greater than $V_{nControl}$ to a final voltage that is less than $V_{nControl} - V_{ls.}$ As the control signal traverses the range defined by voltages V_A and V_B, the switch gate creates an aperture in which the input is coupled to the output for a brief, highly controllable period of time. At all other times, the output is isolated from the input.

† Figure of merit performance measured by repetition rate/aperture width

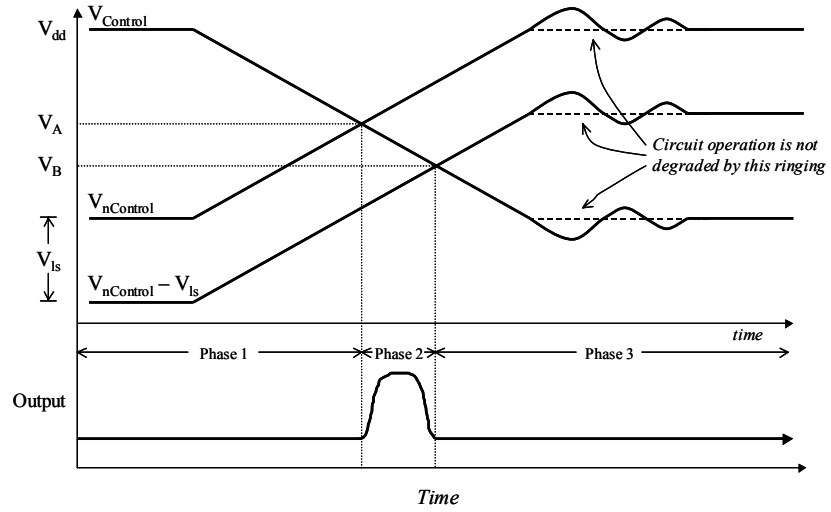

Figure 3 – Sample/Pulse Generation

Unparalleled Noise Rejection and Immunity from Control Signal Imperfections

Isolating the output from the input except as the control signal transitions between the two voltage levels provides the aperture immunity from ringing and other anomalies typically associated with signals at the end of transition. As a result, the Libove Gate exhibits excellent noise rejection on both the input and control signals, and is susceptible to noise only during the brief period of time $V_{Control}$ transitions through $V_{nControl}$ and $V_{nControl} - V_{ls}$. Similarly, the Libove Gate is immune to problems associated with an inadequate slew rate at the beginning of a transition, as this typically occurs before the control signal has slewed sufficiently to reach the initial transition voltage.

Dynamic Control of the Amplitude, Position and Duration of the Sample/Pulse

The Furaxa sampler/pulser permits dynamic modulation of the aperture by increasing or decreasing each of the control voltages. For example, it is possible to make an aperture occur earlier in time by uniformly increasing $V_{nControl}$ and $V_{nControl} - V_{ls}$. In this way, the control signal will transition below $V_{nControl}$ at an earlier time, initiating the aperture sooner. Similarly, the control signal will transition below $V_{nControl} - V_{ls}$ at an earlier time, closing the aperture earlier as well. A wider aperture can also be created by increasing $V_{nControl}$ and decreasing $V_{nControl} - V_{ls}$ so the aperture begins earlier and ends later.

Additionally, a variable duration aperture or pulse is possible with simple manipulation of the control signal, $V_{Control}$. That is, the slope of the control signal determines the duration of the sampling aperture or width of a pulse as illustrated in Figure 4. Since the initiation and extinction of the aperture or pulse are determined independently, the duration of the aperture or pulse can be dynamically selected from a minimum duration, determined by IC device constraints, to a duration of arbitrary length.

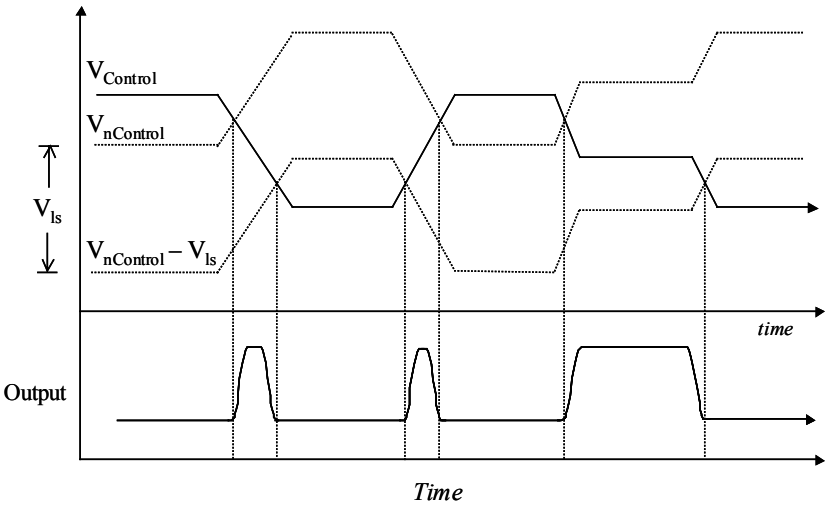

Figure 4 – Sample/Pulse Duration Control

High Speed and Repetition Rate

The absence of carrier-induced charge and discharge time, required by SRD circuits, allows the Libove Gate to achieve very high pulse repetition frequencies. Additionally, the circuit generates an aperture in both transitions of the control signal (low-to-high and high-to-low) permitting two possible samples/pulses per cycle as illustrated in Figure 4. However, if a sample or pulse is desired in only one transition, then the current source may be turned off during the appropriate transition. For example, if an aperture is desired only during the rising edge of $V_{Control}$, the current source can be turned off when the rising edge levels, and turned on again shortly before the next rising edge of the control signal.

Because the Libove Gate circuit can generate two apertures per cycle and is not hampered by the charge and discharge time of SRD circuits, it can operate at better than 2 gigasamples/second – 8x faster than the 250 megasamples/second limit of conventional technology. With 2 Libove Gate circuits, each Furaxa sampler/pulser can achieve 4 gigasamples/second – a 16x improvement over competing sampling/pulsing technology.

Minimal Jitter and Kick-out Voltage

The Libove Gate only requires a single edge of a control signal to open and close an aperture unlike conventional samplers/pulsers. Additionally, the novel circuit architecture minimizes kickout voltage at the input. Together, these features create a circuit with minimal time-jitter as well as superior stability and aperture shape over a range of variables including temperature and IC processes.

High Signal and Control Input Impedances (< 50fF per Sampler/Pulser)

The Libove Gate circuit has high, relatively constant input impedance over the aperture cycle, in contrast to the time-varying input impedance of SRD circuits. Additionally, Furaxa's implementation of the Libove Gate employs true differential inputs and outputs, and does not require feedback level-shifting compensation as do SRD/Schottky samplers. As a result, the Furaxa sampler/pulser benefits from very high CMRR and reduced complexity. Additionally, the input channels are exceptionally robust and resistant to damage from over-voltage, unlike Schottky diode-based circuits.

Easy Integration into Large Arrays of Matched Samplers/Pulsers

Independent and precise adjustment of both aperture position and duration with the Libove Gate enables simple, inexpensive matching of multiple IC components. Additionally, the circuit has much lower excitation power requirements than SRD circuits resulting in far lower thermal drift. Taken together, the power characteristics and precise manipulation of the aperture make it possible to integrate large numbers of tightly matched microwave samplers or pulsers on a monolithic IC. Furthermore, the Libove Gate's immunity to ringing and anomalies in the input and control signals allows a large number of sampler/pulser cells to be driven by a single input signal. With a greater parallel load, the sampler/pulser is less sensitive to degradation of an input waveform than conventional samplers/pulsers.

In addition, the Libove Gate has no extraordinary device requirements such as step-recovery diodes or capacitors. Instead, it utilizes common design elements available across a broad range of IC processes. The Libove Gate can be implemented in any IC process including Gallium Arsenide (GaAs) MESFET, GaAs Heterojunction Bipolar Transistor (HBT), GaAs High Electron Mobility Transistor (HEMT), Indium Phosphide (InP), Silicon-Germanium (SiGe) and Silicon Bipolar or MOS technology. Additionally, the circuit topology allows all transistors to be uniform in type and area allowing an all NMOS/N-channel design requiring no speed-compromising P-channel (or PNP) devices. These features, taken together, provide increased flexibility in implementation, improved performance and substantially reduced cost.

Performance Simulations

The Furaxa sampler/pulser circuit has been comprehensively simulated across a variety of variables including numerous IC processes, noise anomalies and power usage profiles. Simulation results for a single element pulser (Figure 5) and a multi-cell sampling array (Figure 6) are provided using Cadence PSPICE v9.2 and the TriQuint TOM3 model for the TQTRx process.

Single Element Sampler/Pulser

Figure 5 shows simulated output of a single element pulser with eleven different values of pulse amplitude plotted for a differential load consisting of two 50 ohm resistors at 27° Celsius. Voltage for the circuit power supply is +/–5V, and power dissipation is approximately 300mW. Bipolar pulse amplitudes exceeding +/- 500mV are obtained, while preserving the same waveshape and narrow pulse width over the full range of amplitudes.

Figure 5 - Simulation of the Libove Gate Configured as a Pulser

Multi-Cell Sampling Array

Figure 6 illustrates a multi-cell sampling head. Eleven successive samples are simulated on an input waveform that transitions from approximately +450mV to –500mV in 200ps at 27° Celsius. The eleven samples taken during the 20ps time interval labeled "Approximate Aperture Region" are shown as horizontal lines at the right portion of the diagram. The output plots are for a differential load of two 50K ohm resistors in parallel with two 1pf capacitors.

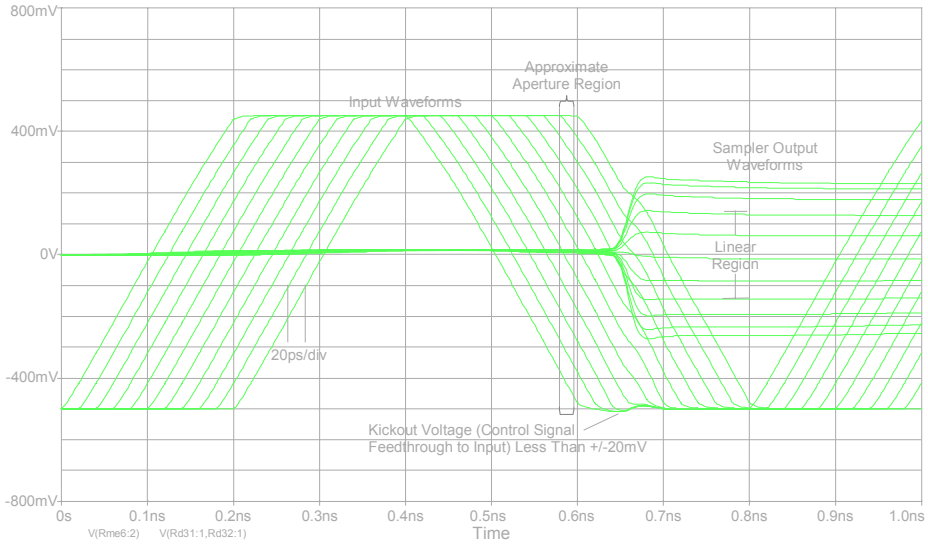

Figure 6 - Simulation of the Libove Gate Configured as a Sampling Head

The results indicate that while the sampling head can accommodate an input signal range of +/-300mV with good linearity, voltages up to +/-450mV can be sampled with some compression. Additionally, input kickout voltage is less than +/-20mV with the negative and positive portions of the waveform each lasting only 30ps. This level of kickout energy is exceptionally low for a sampler of this speed.

Technology Applications

The Libove Gate, by virtue of its scalability to large, tightly matched arrays, significantly advances parallel signal processing in the analog domain and enables next-generation products in a variety of areas including:

Test and Measurement
- High Speed AWGs
- Multi-GHz Single Shot Oscilloscopes
- Time Domain Reflectometers

UWB Communications
- Spectrally tailored Tx/Rx
- Enables complex modulation formats
- Dynamically programmable

High Speed Signal Processing
- Image Reject Mixers with 4 Octave Range
- High speed modulators/demodulators
- Frequency Doublers

High Speed Digital Comms
- Asynchronous counters
- 20 GHz GaAs Prescalers

Optical Communications
- Laser Diode Drivers
- Optical PHYs

Test & Measurement Instrumentation

The advanced performance characteristics of the Furaxa sampler/pulser enable the next-generation of test and measurement instrumentation such as 40+GS/second AWGs and single-shot oscilloscopes with greater than 20GHz analog bandwidth. To realize a 40 GS/second AWG, multiple pulsers can be connected via delay line elements to create an ultra-fast arbitrary waveform generator (Figure 7) in which each of the pulses is controlled in amplitude, position and duration permitting dynamic direct synthesis of complex burst and continuous waveforms. Figure 8 depicts simulated output from this type of pulser array combined with a microprocessor.

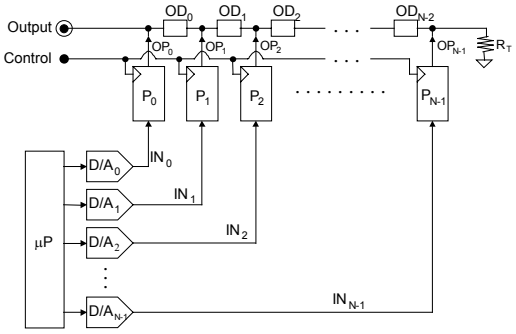

Figure 7 – High Speed Arbitrary Waveform Generator

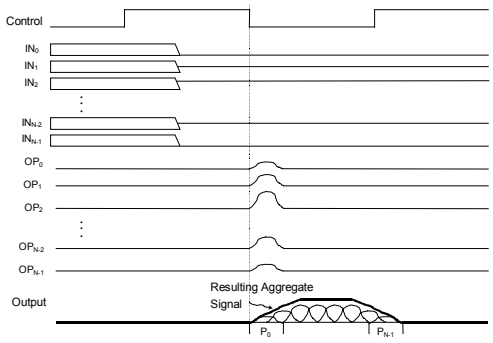

Figure 8 – Waveforms of AWG Circuit in Figure 7

The AWG depicted in Figure 7 has digital to analog converters D/A_0 through D/A_{N-1}, pulsers P_0 through P_{N-1} and a string of analog delay lines OD_0 through OD_{N-2} configured as shown. The D/A converters generate analog voltage levels IN_0 through IN_{N-1} from the digital signals corresponding to the desired shape of waveform. The pulsers then receive analog voltages IN_0 through IN_{N-1} in parallel. Each pulser produces a simultaneous pulse with amplitude proportional to the analog voltage at its respective input terminal.

Figure 8 depicts a simulated waveform of the intermediate signals and the resulting output signal of the generated waveform. Signal OP_0 appears immediately at the Output, while signal OP_1 appears one delay later. Similarly, signal OP_2 appears two delays later, and so on until signal OP_{N-1} appears after N-1 delays. This series of actions results in a very rapid sequence of voltage levels proportional to IN_0 through IN_{N-1} at the output. The flexibility of pulse amplitude, position, and duration allows for a robust "programming" algorithm, increasing the number of possible waveforms that the AWG can generate. Similarly, an arbitrary correlating receiver can be constructed using the Furaxa sampler.

Additionally, Furaxa has designed serial pulser circuits which eliminate the need for delay lines in the AWG circuit illustrated in Figure 7 above. Likewise, serial sampler circuits have also been designed. These serial sampler and pulser ICs will be available in the near future.

Ultra Wideband Communications

The superior operating and matching characteristics of the Furaxa sampler/pulser make it ideally suited for ultra wideband and pulse width modulation applications. The combination of the Libove Gate's stability, repetition rate, aperture modulation, noise rejection and scalability make it ideally suited for advanced UWB applications. A matched UWB transmitter and receiver set incorporating the Furaxa sampler/pulser can do the following:

- Dynamically synthesize and receive complex signals in a 25 GHz band
- Control Tx spectral signature
- Adapt to changing spectrum conditions
- Eliminate the need for Tx filters because it is directly band-limited
- Pre-correct antenna Tx/Rx
- Adapt to changing FCC regulations through dynamic programming

In short, a Furaxa sampler/pulser array generates faster and more complex pulse/sample structures at a lower cost than possible with conventional technology. Additionally, the Furaxa pulser allows the UWB system to dynamically control its spectral signature and adapt to changing spectrum conditions to mitigate effects such as rain fade. Moreover, a UWB system incorporating the Furaxa sampler/pulser has the added advantage of being directly band-limited at the point of synthesis and avoids out-of-bound interference with existing spectrum users. Finally, because the Furaxa IC is programmable, it can even be adapted to changing FCC regulations – saving thousands of dollars of capital equipment from obsolescence.

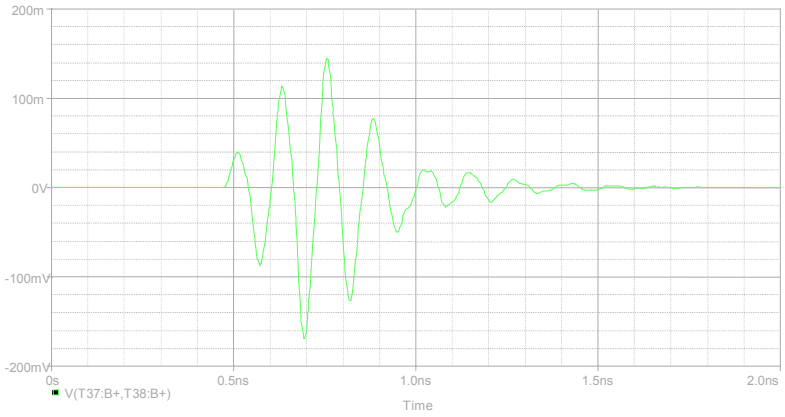

Figure 9 – Directly Synthesized Gaussian-Envelope UWB Pulse

Figure 9 demonstrates the flexibility of the pulser cell. A modulated Gaussian envelope pulse is generated with precise amplitude and duration control. A similar spectrally tailored signal can be used in a secure UWB network having negligible transmitted signal energy below 3GHz with 20GHz of effective bandwidth. This type of system would effectively eliminate concerns of interference with GPS and aircraft communications systems without the need for filters.

Finally, the Furaxa sampler/pulser enables efficient modulation schemes to be employed which significantly enhance the bandwidth efficiency of any UWB system. Schemes such as Quadrature Pulse Amplitude Modulation are beyond the capability of conventional sampler/pulser technology at these frequencies, but are made possible with the Furaxa sampler/pulser.

High Speed Analog Signal Processing

The operating characteristics of the Furaxa sampler/pulser also make it an ideal building block in new ICs capable of parallel processing a large number of rapidly-acquired or synthesized samples enabling more complex and more accurate real-time synthesis and processing than was formerly possible. New architectures in signal processing, amplification, data separation, equalization, mixing and filtering are now economically practical to develop. For example, the Furaxa sampler/pulser can be used as an element in complex high-speed modulators and demodulators, image reject mixers and frequency doublers.

Figure 10 illustrates a generalized signal processing architecture for a wide variety of frequency mixers and modulators, correlators, microwave amplifiers, filters, Viterbi and other convolutional decoders, and almost any other linear and non-linear signal processing system at high frequencies. The architecture consists of an input terminal coupled to a string of analog delay lines, ID_0 through ID_{N-2}, with the output of ID_0 coupled to a terminating resistor R_{TI}. The outputs of the delay lines, each containing a copy of the input signal delayed by a sequentially increasing amount, are coupled into samplers, S_0 through S_{N-1}. On each falling edge of the control signal, each sampler takes a snapshot of the input generating samples IS_0 through IS_{N-1}. These samples are coupled into low-speed or medium-speed circuitry which performs the desired signal processing operations on the data from the samplers. The outputs generated by the low/medium speed signal processing circuitry are coupled to pulse generators, P_0 through P_{N-1}. The pulse generators take a simultaneous snapshot of the output of the signal processing circuitry on each falling edge of the control signal and generate simultaneous pulses, OP_0 through OP_{N-1}, that are proportional in amplitude to

their respective output of the signal processing circuitry. The pulse output of P_0 through P_{N-1} is coupled to a string of delay lines, OD_0 through OD_{N-2}, which create a continuous waveform consisting of N sequential voltage values each lasting the length of one delay line.

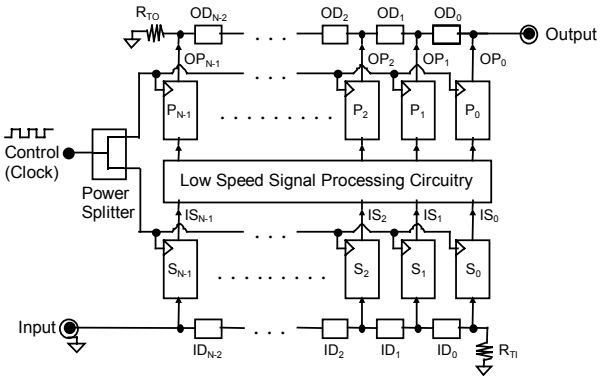

Figure 10 - Example of an Ultra High-Speed Signal Processing System using the Libove Gate

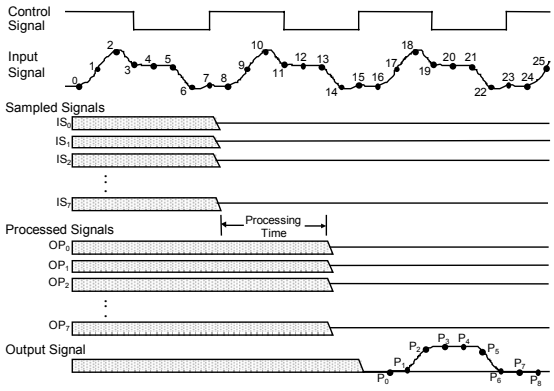

Figure 11 – Waveforms of Circuit in Figure 9 for a Channel Equalizer with N=7

In this way, the circuit breaks down a continuous waveform into a sequence of N rapidly acquired time samples, each of which can be processed at a rate that is N times slower. The result is transformed back into a sequence of N very rapidly changing output samples. Every time the control signal makes a transition in one direction a new set of samples are taken, processed, and converted into an output stream as illustrated in Figure 11.

While the concept of taking a rapid sequence of samples, holding them for a period of time, processing them in parallel, and then re-serializing the result of these parallel outputs is not novel, the architecture of the Libove Gate makes signal processing practical for much faster signals than formerly possible. For example, conventional microwave image-reject mixers used to convert an RF signal into a near-baseband signal typically have less than an octave in bandwidth over which they can operate. In contrast, the circuit architecture described above would produce an advanced image reject mixer with a frequency range of several octaves that could operate at much higher frequencies. Similarly, faster active filters and amplifiers with better linearity and flatter frequency response are now feasible.

High-Speed Digital Communications

The Libove Gate can also be used in ultra-fast digital switching elements. Though limited in scope, the technology lends itself to very high-speed digital applications such as prescalers and asynchronous counters.

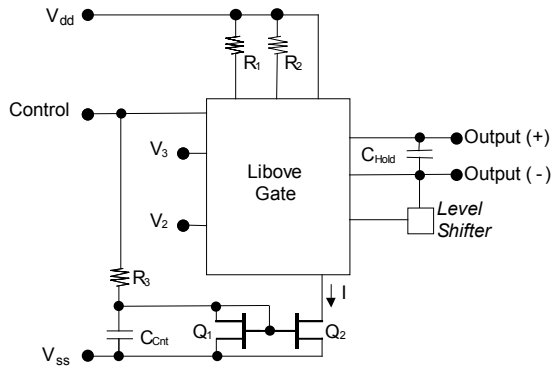

Figure 12 – Toggle Flip-Flop Implementation

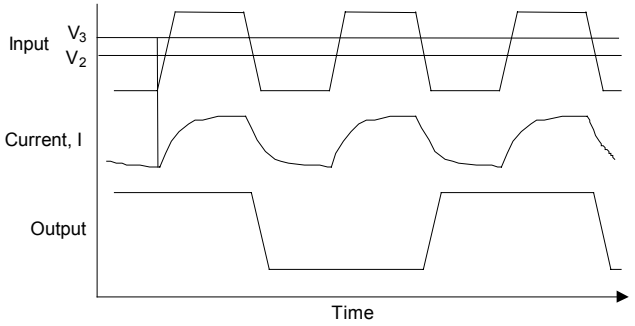

Figure 13 – Toggle Flip-Flop Implementation

Figure 12 illustrates a toggle-type flip-flop capable of acting as a prescaler at frequencies in excess of 20 gigaHertz. The inverting output of the sampler/pulser circuit is connected, via two conventional level shifters, to its non-inverting input terminal, and vice versa.

Figure 13 illustrates a waveform diagram of the operation of the toggle-type flip-flop circuit in Figure 12. As long as the transition time of the control signal from V_3 to V_2 is shorter than the delay time from the input terminals to the output terminals of the sampler, the circuit will toggle on every second negative transition of the control signal. This will produce an output frequency that is one-half of the input frequency as shown in Figure 13.

It should be noted that the current source is turned on and off using a delayed version of the control signal, so that the flip-flop does not sample the inputs on the rising edge of the control signal, but only on the falling edge. In this way, the circuit correctly divides by two. Also, since the output is held by a hold capacitor, its value will sag over time, at a time constant equal to $(R_1+R_2) \times C_{hold}$. For this reason, the circuit should not be operated at a frequency below approximately $1 /[2 \times (R_1+R_2) \times C_{hold}]$.

Optical Communications

Currently, high-speed optical channels are often distorted by dispersion and high-frequency attenuation that smear the impulse response of the communication link and require channel equalizers to optimize performance. Conventional technology is prohibitively costly and too complex to implement an optimal equalizer architecture. As a result inferior methods are currently used. However, the Libove Gate is significantly less costly and easier to implement than conventional technology permitting the optimal architecture to be employed to produce superior performance.

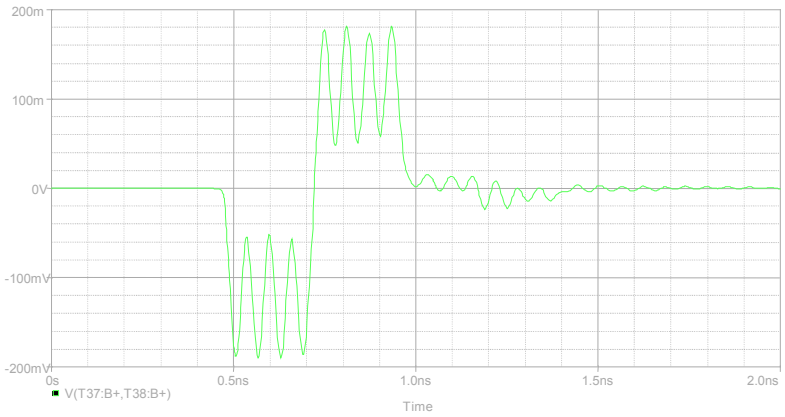

Figure 14 – Directly Synthesized Pulse Train for Optical SERDES

Figure 14 displays a sequence of 4 negative pulses followed by 4 positive pulses. This direct synthesis/sampling capability can form the basis of a low-power, inexpensive 40Gb/s optical SERDES. On the receive side, the technology can be employed to allow high-speed clock/data recovery with no phase-lock preamble necessary leading to corresponding increases in network efficiency.

Figure 15 illustrates an example of an improved equalizer architecture enabled by the Furaxa sampler. The input signal is coupled into a string of analog delay lines, ID_0 through ID_{N-2}, and the first sampling cell of a string of samplers, S_0 through S_{N-1}. The output from each successive delay line is coupled into its respective sampling cell, S_1 through S_{N-1}. A control signal generated by a phase locked loop is coupled into each of the samplers. The delayed input signals are sampled simultaneously so that an entire cycle of an input waveform is captured. Then, the samples of the input waveform can be processed with slower, more precise parallel blocks of circuitry.

For example, an array of analog multipliers multiplies the samples of the input signal waveform by a series of analog coefficients K_0 through K_{N-1}. The output of each of these multipliers is coupled into a respective delay line, OD_0 through OD_{N-2}. From the delay line OD_{N-2}, an equalized output is generated which is a weighted sum of the sampled input signal at N different past times. In this way, a conventional Finite Impulse Response (FIR) filter is created. The coefficients K_0 through K_{N-1} can be generated by a conventional microprocessor-based system including a conventional single sampling gate formed by a low speed multi-channel sample and hold and a multiplexer, an analog-to-digital (A/D) converter, a microprocessor with a parallel data output and multiple digital-to-analog (D/A) converters to convert each parallel data output into the analog coefficients K_0 through K_{N-1}.

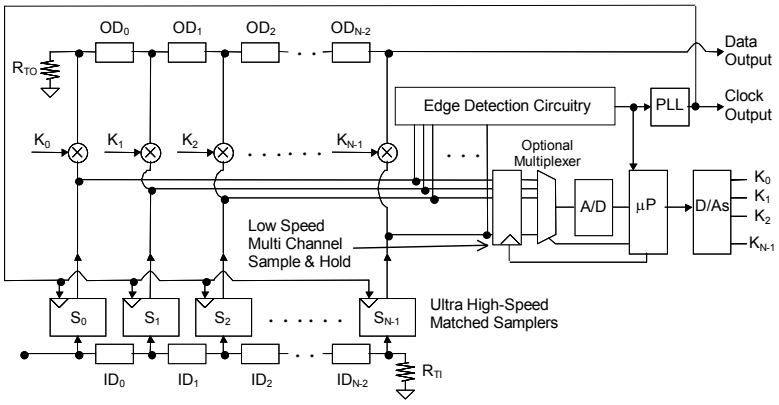

Figure 15 – Improved FIR Equalizer Using Multiple Ultra-Fast Samplers

The circuitry in Figure 15 captures a single snapshot of a large number of points on the input waveform. This permits a complete cycle of an input waveform to be held in a conventional, relatively slow multi-channel sample-and-

hold that can then be read at leisure by the microprocessor. The microprocessor can compute coefficients K_0 through K_{N-1} to implement an inverse filter which can compensate for the degradation that has occurred in a communications channel. The very high speed and tight matching of the precisely timed sequence of sampling apertures enables more intricate processing of portions of a high frequency waveform than was formerly feasible.

Additionally, the edge detection circuitry can alternatively be connected to the outputs of the low-speed multipliers in the signal processing system illustrated in Figure 10 with an output coupled to the phase-locked loop. The edge detection circuit can determine the boundaries of each bit cell on a cell-by-cell basis, enabling more frequent boundary delineation and consequently more accurate generation of a clock waveform in the middle of each bit cell. The ability to more quickly extract a clock waveform from the raw signal is critical in communications systems which require very rapid synchronization to an incoming data stream.

Enabling the Next Wave of Development and Innovation

The Libove Gate represents no less than a leap forward in sampling/pulsing technology. The novel circuit architecture provides:

- Unparalleled noise rejection and immunity from control signal imperfections
- Dynamic control of the amplitude, position and duration of the sample/pulse
- Minimal jitter and kick-out voltage
- High signal and control input impedances
- Easy integration into large arrays of matched samplers/pulsers
- Fully differential inputs and outputs

The embodiment of the Libove Gate in the Furaxa sampler/pulser produces a minimum 8x figure of merit performance improvement and 16x increase in the aperture repetition rate of the leading conventional technology. In short, the exceptional set of performance characteristics of the Furaxa sampler/pulser makes it uniquely suited for use in advanced test and measurement instrumentation, ultra wideband communications, high speed analog signal processing, advanced optical communications and high speed digital processing.

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